

WHAT IS CLAIMED IS:

1           1.    A process for forming at least one portion of a  
2    compound material formed from elements of an initial  
3    material and of a metal within an electronic circuit,  
4    comprising the following steps:  
5           (a) formation of a cavity that includes at least one  
6    opening onto an access surface and has an internal wall  
7    having at least one region of initial material;  
8           (b) deposition of the metal close to said region of  
9    initial material;  
10          (c) heating of the circuit so as to form a portion of  
11    compound material in said region of initial material; and  
12          (d) removal of at least one portion of the metal that  
13    has not formed some of the compound material from the  
14    cavity via said opening.

1           2.    The process according to Claim 1, wherein step  
2    (a) comprises the removal of at least one material from the  
3    circuit.

1           3.    The process according to Claim 1, wherein step  
2    (a) comprises the transfer of at least one material from

3 a temporary substrate to a final substrate carrying the  
4 electronic circuit.

1 4. The process according to Claim 1, wherein the  
2 initial material comprises silicon, germanium, arsenic,  
3 selenium, or a mixed compound comprising at least one of  
4 the above elements.

1 5. The process according to Claim 1, wherein step  
2 (b) comprises introducing the metal into the cavity via the  
3 opening so as to form a deposition of the metal on at least  
4 said region of initial material.

1 6. The process according to Claim 1, wherein step  
2 (b) comprises depositing the metal outside the cavity close  
3 to said opening and wherein, during step (c), the metal  
4 diffuses into the cavity, via said opening of the cavity,  
5 as far as said region of initial material, so as to form  
6 a portion of the compound material in said region of  
7 initial material.

1           7.    The process according to Claim 1, wherein step  
2   (b) comprises a chemical deposition of the metal from  
3   gaseous precursor compounds incorporating atoms of the  
4   metal, or a deposition using a liquid solution introduced  
5   into the cavity and incorporating dissolved chemical  
6   compounds based on the metal in an oxidized form.

1           8.    The process according to Claim 1, wherein the  
2   metal comprises cobalt, tantalum, tungsten, titanium,  
3   aluminium, copper, silver, platinum, nickel or an alloy  
4   comprising at least one of the above metals.

1           9.    The process according to Claim 1, wherein the  
2   compound material formed is electrically conducting.

1           10.   The process according to Claim 1, wherein step  
2   (d) comprises an etching by means of a solution including  
3   chemical reactants.

1           11.   The process according to Claim 1, wherein, during  
2   step (c), substantially all the initial material present

3     in said region of initial material is converted into  
4     compound material.

1           12. The process according to Claim 1, wherein the  
2     internal wall of the cavity has at least two regions of  
3     initial material separated by an intermediate region of a  
4     material other than the initial material and wherein,  
5     during step (c), the initial material of at least one of  
6     said regions of initial material is made to diffuse into  
7     the metal so as to form a portion of compound material  
8     connecting said regions of initial material.

1           13. The process according to Claim 1, wherein the  
2     internal wall of the cavity has a region of silica or of  
3     silicon nitride.

1           14. The process according to Claim 1, wherein the  
2     cavity comprises a cylindrical or parallelepipedal first  
3     volume open to the access surface.

1           15. The process according to Claim 14, wherein the  
2     cavity furthermore comprises a second volume into which the

3 first volume runs on the opposite side from the access  
4 surface, the second volume extending further than the first  
5 volume parallel to the access surface.

1 16. An electronic circuit including a portion of  
2 compound material manufactured by the process of Claim 1.

1 17. The electronic circuit according to Claim 16,  
2 wherein the portion of compound material comprises at least  
3 one electrical connection.

1 18. An MOS transistor including a gate having a  
2 portion of compound material manufactured by the process  
3 of Claim 1.

1 19. The MOS transistor according to Claim 18, wherein  
2 the compound material has a work function within a range  
3 of  $\pm 25\%$  around a mean value of two work functions of a p-  
4 type semiconductor material and an n-type semiconductor  
5 material, respectively.

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PATENT APPLICATION  
Docket #61919/10uspx

1           20. An electronic circuit including an MOS transistor  
2    having a gate with a portion of compound material  
3    manufactured by the processing of Claim 18.

1           21. A process for MOS transistor gate formation,  
2    comprising the steps of:  
3           depositing a temporary material;  
4           forming a transverse structure including a silicon bar  
5    doped to define source, drain and channel regions;  
6           removing the temporary material from under the  
7    transverse structure to define a cavity;  
8           depositing a metal on exposed surfaces of the  
9    transverse structure and in the cavity; and  
10          heating to convert the portions of the silicon bar  
11    adjacent to deposited metal into silicide.

1           22. The method of claim 21 further including removing  
2    the deposited metal which is not converted to silicide by  
3    heating.

1           23. The method of claim 21 wherein heating converts  
2    certain portions of the silicon bar to define source and  
3    drain electrical contacts of the transistor.

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1           24. The method of claim 21 wherein heating converts  
2   certain portions of the silicon bar to define a gate  
3   surrounding the channel region.

1           25. The MOS transistor formed by using the method of  
2   claim 21.



1           26. A process for producing electrical connections  
2   between separate circuit portions, comprising:  
3           defining first and second separate silicon portions;  
4           depositing a metal overlying the first and second  
5   separate silicon portions and a structure therebetween; and  
6           heating to convert portions of the first and second  
7   silicon portions adjacent to deposited metal into silicide,  
8   wherein the silicide from the first and second silicon  
9   portions connects.

1           27. The process of claim 26 wherein the first and  
2   second separate silicon portions may be vertically  
3   separated.

1           28. The process of claim 26 wherein the first and  
2   second separate silicon portions may be horizontally  
3   separated.

1           29. The process of claim 26 further including:  
2           forming a temporary material adjacent the first and  
3           second separate silicon portions;  
4           burying the temporary material and first and second  
5           separate silicon portions with a covering material;  
6           forming a chimney through the covering material to  
7           reach the temporary material; and  
8           removing the temporary material through the chimney  
9           to form a cavity.

1           30. The process of claim 29 wherein depositing  
2           comprises depositing the metal through the chimney to at  
3           least partially fill the cavity.

1           31. The method of claim 26 further including removing  
2           the deposited metal which is not converted to silicide by  
3           heating.

1           32. The electrical connection formed by using the  
2           method of claim 26.